REMARKS

Applicants thank the Examiner for the very thorough consideration given the present application.

Claims 1-21 are now present in this application. Claims 1, 10 and 21 are independent.

Claims 1, 10 and 21 have been amended. Reconsideration of this application, as amended, is respectfully requested.

Priority Under 35 U.S.C. § 119

Applicants thank the Examiner for acknowledging Applicants' claim for foreign priority under 35 U.S.C. § 119, and receipt of the certified priority document.

Information Disclosure Citation

Applicants thank the Examiner for considering the references supplied with the Information Disclosure Statement filed December 3, 2001, and for providing Applicants with an initialed copy of the PTO-1449 form filed therewith.

Drawings

Applicants thank the Examiner for indicating that the drawings filed on December 3, 2001 have been accepted by the Draftsperson.

Rejection Under 35 U.S.C. § 102

Claim 21 stands rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,025,254 to Doyle et. al. (Doyle). This rejection is respectfully traversed.

A complete discussion of the Examiner's rejection is set forth in the Office Action, and is not being repeated here.

Doyle discloses a method of forming a *first* silicide layer 110 concurrently with the formation of the source/drain silicide layer (see Doyle, Col.2, lines 53-55). It is clear from the resulting structure (see Fig.1a) that the metallic layer used to form the silicide has been etched away.

Therefore, Doyle fails to disclose forming a first silicide pattern on the non-silicide gate without etching a silicide from which the silicide pattern is fabricated, as recited in independent claim 21, as amended. Reconsideration and withdrawal of this art grounds of rejection are respectfully requested.

Rejections under 35 U.S.C. § 103

Claims 1-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Doyle in view of Broadbent et al. (IEEE Transactions on Electron Devices Vol. 36.No.11, November 1989). This rejection is respectfully traversed.

A complete discussion of the Examiner's rejection is set forth in the Office Action, and is not being repeated here.

Doyle discloses a gate electrode layer 104, formed of polysilicon, and sidewall spacers 108 which are formed adjacent to gate electrode layer 104 (see Figs. 1a-1e). Figure 1(b) shows the deposition of a sacrificial dielectric layer 114 over sidewall spacers and silicide layer 110. The surfaces of gate 104 make no contact with layer 114. Hence, dielectric layer 114 is not formed on surfaces of the gate. Particularly, Doyle does not disclose or suggest forming an insulating film thicker than the gate on said exposed top and side surfaces and on an entire surface of the substrate, as recited in independent claim 1, as amended, and similarly stated in independent claim 10 (as amended). Broadbent et al. cannot fill this vacancy.

Claims 2-9 and 11-20 depend, either directly or indirectly on independent claims 1 and 10. Since neither Doyle, nor Broadbent et al. discloses or suggest forming an insulating film thicker than the gate on said exposed top and side surfaces and on an entire surface of the substrate, Doyle

in view of Broadbent et al. cannot render claims 1-20 obvious to one of ordinary skill in the art. Reconsideration and withdrawal of this art grounds of rejection are respectfully requested.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone Percy L. Square, Registration No. 51,084, at (703) 205-8034, in the Washington, D.C. area.

Prompt and favorable consideration of this Amendment is respectfully requested.

Attached hereto is a marked-up version of the changes made to the application by this Amendment.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By: _____

Joseph A. Kolasch
Reg. No.: 22,463
P.O. Box 747
Falls Church, Virginia 22040-0747
Telephone: (703) 205-8000

JAK/PLS:mlr:asc

Attachment: Version with Markings to Show Changes Made

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

The claims have been amended as follows:

1. (Amended) A method for forming a gate in a semiconductor device, comprising:

forming a first insulating film and a non-silicide conductive film on a semiconductor substrate;

patterning the first insulating film and the conductive film, to form a gate, wherein the top and side surfaces of said gate are exposed;

forming a second insulating film thicker than the gate on said exposed top and side surfaces and on an entire surface of the substrate;

planarizing the second insulating film, to again expose the top surface of the gate;

depositing a refractory metal layer on an entire surface such that the refractory metal layer is adjacent to the patterned conductive film;

forming a silicide layer on an upper surface of the gate by heat treatment; and

etching the refractory metal layer and the second insulating film.

10. (Amended) A method of fabricating a gate in a semiconductor device, comprising:

forming a non-silicide conductive film [pattern] on a semiconductor substrate; [and]

patterning the conductive film, to form a gate, wherein the top and side surfaces of said gate are exposed;

forming an insulating film thicker than the gate on said exposed top and

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side surfaces and on an entire surface of the substrate;

planarizing the second insulating film, to again expose the top surface of the gate; and

forming a silicide pattern on the conductive pattern, the silicide pattern having a predetermined width, and being formed after the conductive pattern is formed, said step of forming a silicide pattern comprising:

forming a refractory metal on the conductive pattern such that the refractory metal is adjacent to the conductive pattern; and

heat treating the refractory metal to form the silicide pattern having the predetermined width at an intersection between the refractory metal and the conductive pattern.

21. (Amended) A method of fabricating a gate electrode of a predetermined width, comprising:

forming a gate insulating layer and a non-silicide gate on a semiconductor substrate; and

forming a first silicide pattern on the non-silicide gate [insulating layer] without etching a silicide from which the silicide pattern is fabricated.